Integrated Circuits and Operational Amplifiers

designing an active circuit. As active devices can be easily fabricated in ICs, it is usually possible to get rid of the inductors altered

The monolithic IC form of the simple circuit of Fig. 14.1 has already been shown in Fig. (e). Another example is about 15 per shown in Fig. 14.1 has already been shown in Fig. 14.1 has already been shown in Fig. (e). 14.2 (e). Another example is shown is Fig. 14.3A which incorporates circuit components like a diode (D), a resistor (B)diode (D), a resistor (R), an npn transistor (T), and a capacitor (C). The circuit is shown in Fig. 14.3A (a) whose manufactor (T), and a capacitor (C). Isolation between the Fig. 14.3A (a) whose monolithic IC layout is depicted in Fig. 14.3A (b). Isolation between the components is achieved by see components is achieved by connecting the p-type substrate to the most negative voltage. The pn junctions separating the accuracy of the property of the position of the property of the position of the positi junctions separating the components are then reverse biased, offering a dc isolation resistance higher than 10 MO higher than 10 M Ω .

14.4 LIMITATIONS OF ICS

- (i) Very small resistors (less than a few ohms) and very large resistors(of the order of meg ohm) cannot be obtained by the IC technology.
- (ii) Large capacitances (greater than 200 pF) cannot be produced.
- (iii) Inductors and transformers cannot be fabricated in the IC.
- (iv) The tolerance of the IC passive components is large (typically \pm 20 per cent).
- (v) The IC components are voltage-sensitive and have large temperature coefficients.
- (vi) The performance of the *p-n-p* transistor is poor.
- (vii) The power dissipation capacity is small.
- (viii) The high-frequency performance of ICs is limited by the parasitic capacitances.

With the progress in technology, some of these limitations are expected to be removed in

14.5 OPERATIONAL AMPLIFIERS

The operational amplifier (abbreviated OP AMP) is the best known example of a general-purpose linear integrated circuit. The IC OP AMP was developed by Robert Widlar in 1964. Basically, the OP AMP is a direct-coupled high-gain differential-input amplifier. The significance of the term 'operational' is that the OP AMP can perform mathematical operations such as summation, subtraction, integration, and differentiation. Such operations are important in analog computers. In addition, the OP AMPs can be used in signal amplification, wave forming, servocontrols, impedance transformation, active filters, oscillators, voltage regulators, analog-to-digital and digital-to-analog converters, to mention but a few. IC OP AMPs are useful in communication equipment, instrumentation, and data processing.

The advantage of OP AMPs is that negative feedback can be applied. The performance of the OP AMP with negative feedback is controlled by the feedback elements independent of the characteristics of the transistors and other elements that constitute the OP AMP. As the feedback elements are usually passive, the circuit operation is very stable and predictable. The IC OP AMPs are inexpensive and have temperature stabilisation. The user of the device need not know the detailed internal circuit configuration of the OP AMP. He simply needs to be acquainted with its terminal properties, so that by connecting external circuit components he can use the OP AMP for a specific purpose.

Circuit Symbol: Figure 14.4 shows the circuit representation of an operational amplifier. It has two input terminals (marked a and b) and one output terminal (marked c). Terminal a is known as the inverting input terminal and is labelled '-'. The significance of the negative sign is

that a signal applied at the terminal a appears at the terminal c with its polarity reversed. Terminal b is called the *noninverting* input terminal and is labelled '+'. A signal applied to the terminal b appears at the terminal c with the same polarity. The output voltage at c is proportional to the difference of the two signal voltages applied at the two input terminals simultaneously. The constant of proportionality gives the openloop voltage gain (A) of the operational amplifier. A is a real constant, and for an ideal amplifier A approaches infinity for all frequencies.

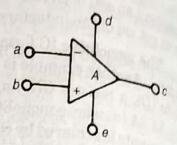


Fig. 14.4 Circuit symbol of a basic OP AMP.

The power supply voltages which are usually balanced with respect to ground are applied The power supply voltages which are defined to the terminals d and e are, however, often omitted in schematic to the terminals d and e. The terminals d and e are, however, often omitted in schematic circuits.

OP AMP Characteristics: The ideal OP AMP has the following properties:

- 1. An infinite voltage gain.
- 2. An infinite input impedance.
- 3. Zero output impedance.
- 4. An infinite bandwidth.
- 5. Characteristics not drifting with temperature.
- 6. Perfect balance, i.e. the output voltage is zero when equal voltages are applied to the two input terminals.

For a practical OP AMP, the dc or the low-frequency voltage gain is typically 103 to 106. The bandwidth is finite, the voltage gain being constant up to several hundred kilohertz and then decreasing with increase in frequency. The input impedance is between 150 kiloohm and a few hundred meg ohm. The output impedance lies in the range 0.75 to 100 ohm. The practical OP AMPs do not have a prefect balance and their characteristics also change somewhat with temperature.

Common-mode rejection ratio. An OP AMP is basically a differential amplifier with signal voltages v_1 and v_2 each measured with respect to ground, applied to the noninverting terminal b and the inverting terminal a respectively (Fig. 14.4). The output voltage appearing at the terminal c is v_0 , measured with respect to ground. In practice, the difference signal

 $v_d = v_1 - v_2$ and also the average signal, called the common-mode signal $v_c = \frac{v_1 + v_2}{2}$ are amplified to produce the output voltage. We have

$$v_0 = A_1 v_1 + A_2 v_2 \tag{14.1}$$

where A_1 is the voltage gain when the terminal a is grounded and A_2 is that when the terminal

$$v_1 = v_c + \frac{1}{2} v_d \tag{14.2}$$

and

$$v_2 = v_c - \frac{1}{2}v_d \tag{14.3}$$

Using Eqs. (14.2) and (14.3) in (14.1) we get

$$v_0 = \frac{1}{2} (A_1 - A_2) v_d + (A_1 + A_2) v_c = A_d v_d + A_c v_c$$
 (14.4)

$$A_d = \frac{1}{2} (A_1 - A_2) \tag{14.5}$$

$$(14.6)$$

 A_d is the voltage gain for the difference signal and A_c is that for the common-mode signal. In the ideal case, A_d is infinitely large while A_c is zero. In practice, the situation is not truly ideal, and a figure of monit, called the $A_c = A_1 + A_2$ ideal, and a figure of merit, called the common-mode rejection ratio (CMRR) of the OP AMP has to be introduced. It is defined by

$$CMRR = \left| \frac{A_d}{A_c} \right|. \tag{14.7}$$

Since A_d needs to be large and A_c very small, the amplifier must be so designed that the CMRR is much larger than unity.

Offset error voltages and current: An ideal OP AMP is perfectly balanced, i.e. $v_0 = 0$ when $v_1 = v_2$. In practice, an OP AMP shows an unbalance due to a mismatch of the built-in transistors following the inverting and the noninverting input terminals. This mismatch gives unequal bias currents flowing through the input terminals. Thus an input offset voltage has to be applied between the two input terminals to balance the output.

The input bias current is half the sum of the individual currents entering the two input terminals of a balanced amplifier [Fig. 14.5(a)]. The input bias current is

$$i_B = \frac{i_{b1} + i_{b2}}{2}$$
, when $v_0 = 0$.

The input offset current i_{i0} is the difference between the individual currents entering the input terminals of a balanced amplifier [Fig. 14.5(a)]. Thus

$$i_{i0} = i_{b1} - i_{b2}$$
, when $v_0 = 0$.

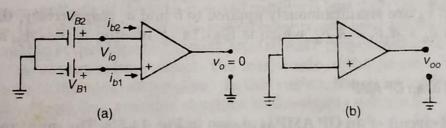


Fig. 14.5 (a) Input offset voltage (b) Output offset voltage.

The input offset voltage v_{i0} is the voltage to be applied between the input terminals to balance the amplifier [Fig. 14.5(a)].

The output offset voltage v_{00} is the voltage at the output terminal when the two input terminals are grounded [Fig. 14.5(b)].

Practical OP AMPs have arrangements to balance the offset voltage.

14.6 CIRCUIT OF AN OP AMP

The circuit of a general-purpose monolithic IC OP AMP is shown in Fig. 14.5A. The high input impedance is provided by the Darlington connection of two npn transistors. There are two differential gain stages; the output is taken from a single-ended emitter follower. The transistors T_1 and T_2 are identical; so are the transistors T_3 and T_4 . Also, $R_1 = R_2$. The errors from the thermal drift are reduced, since the corresponding components of each pair are affected almost equally owing to their close spacing in the IC chip.

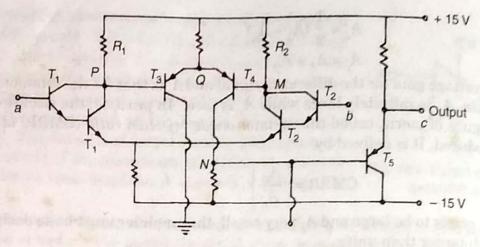


Fig. 14.5A Circuit of an IC OP AMP.

Let the inverting input terminal a be grounded and a small positive voltage v_1 be applied to the noninverting input terminal b. This will drop the potential of the point M, so that T_4 will conduct more. The potential of the point N increases consequently. The transistor T_5 now conducts less, so that the output voltage (at the terminal c) becomes more positive. Thus a signal applied to b appears with the same polarity (though amplified) at c. If A_1 is the voltage gain, the output voltage is $v_0 = A_1v_1$. Since v_0 and v_1 have the same polarity, A_1 is positive.

Now, let b be grounded and a small positive voltage v_2 be applied to a. The point P becomes less positive, so that T_3 conducts more. As a result, the potential of the point Q falls and T_4 conducts less. The potential of N thus becomes more negative, so that T_5 conducts more. The potential of the output terminal c thus falls. So, a signal applied to a appears in an amplified form with its polarity reversed at c. If A_2 is the voltage gain, we have for the output voltage, $v_0 = A_2 v_2$. Since v_0 and v_2 have opposite polarity, A_2 is negative.

When v_1 and v_2 are simultaneously applied to b and a, respectively, the output voltage can be written as $v_0 = A_1v_1 + A_2v_2$, which is Eq. (14.1). Ideally, $A_1 = -A_2$, so that we obtain $v_0 = 0$ for $v_1 = v_2$.

AC equivalent circuit of an OP AMP

The AC equivalent circuit of an OP AMP is shown in Fig. 14.5B. The input resistance between the inverting input terminal and ground is R_{ia} , that between the noninverting input terminal

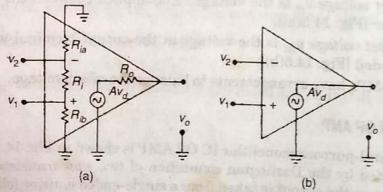


Fig. 14.5B AC equivalent circuit of an OP AMP: (a) practical, (b) ideal.

and ground is R_{ib} , and that between the two input terminals is R_i . All the three resistances R_{ib} , R_{ib} and R_i are typically very high. The output voltage is the amplifier gain A multiplied by the

where
$$A_d = \frac{1}{2} (A_1 - A_2)$$
 (14.5)
and $A_c = A_1 + A_2$ (14.6)

 $A_c = A_1 + A_2$ A_d is the voltage gain for the difference signal and A_c is that for the common-mode signal. In the ideal case, A_d is infinitely large while A_c is zero. In practice, the situation is not truly ideal, and a figure of merit, called the common-mode rejection ratio (CMRR) of the OP AMP has to be introduced. It is defined by

$$CMRR = \left| \frac{A_d}{A_c} \right| . (14.7)$$

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The input bias current is half the sum of the individual currents entering the two input terminals of a balanced amplifier [Fig. 14.5(a)]. The input bias current is

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, when $v_0 = 0$.

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$$i_{i0} = i_{b1} - i_{b2}$$
, when $v_0 = 0$.

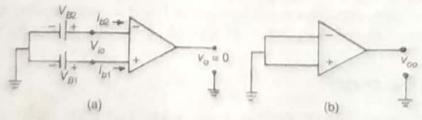


Fig. 14.5 (a) Input offset voltage (b) Output offset voltage.

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an OP AMP being infinite, no current can flow into the OP AMP through the virtual ground. So a virtual ground cannot serve as a sink for current.

The current i through the resistance R_1 is

$$i = \frac{v_1 - v}{R_1} \tag{14.8}$$

Assuming that the OP AMP is an ideal one with an infinite input impedance, the current i passes through R_f and not into the OP AMP. Kirchhoff's current law at the point G gives

$$\frac{v_1 - v}{R_1} = \frac{v - v_0}{R_f} \tag{14.9}$$

As the point G is a virtual ground, $v \approx 0$. Hence Eq. (14.9) reduces to

$$\frac{v_1}{R_1} = -\frac{v_0}{R_f} \tag{14.10}$$

The ratio of the output voltage v_0 and the input voltage v_1 is the closed-loop gain of the amplifier. So, the closed-loop gain of the inverting amplifier is

$$\frac{v_0}{v_1} = -\frac{R_f}{R_1} \tag{14.11}$$

Thus the closed-loop voltage gain is the ratio of the feedback resistance R_f to the input resistance R_1 . The negative sign signifies that the output voltage is inverted with respect to the input voltage.

The input resistance of the amplifier system is

$$R_{in} = \frac{v_1}{i} = \frac{v_1}{(v_1 - v)/R_1} \approx R_1 \tag{14.12}$$

using Eq. (14.8) and noting that $v \approx 0$. It should be noted that R_{in} refers to the entire amplifier system and not to the OP AMP which has an infinite input impedance. The output resistance of the inverting amplifier is very small.

2. Phase shifter: Let the resistances R_1 and R_f in the circuit of Fig. 14.6 be replaced respectively by the impedances Z_1 and Z_f which have equal magnitudes but different phase angles. Hence

$$\frac{v_0}{v_1} = -\frac{Z_f}{Z_1} = -\frac{|Z_f| \exp(j\theta_f)}{|Z_1| \exp(j\theta_1)} = \exp[j(\pi + \theta_f - \theta_1)]$$
 (14.13)

Since $|Z_f| = |Z_1|$ and $\exp(j\pi) = -1$. The angles θ_f and θ_1 are respectively the phase angles of Z_f and Z_1 . Equation (14.13) shows that v_0 leads v_1 by $(\pi + \theta_f - \theta_1)$, but $|v_0| = |v_1|$. Obviously, the circuit shifts the phase of a sinusoidal input voltage leaving its magnitude unaltered. The phase shift can be anything between 0° and 360°.

3. Scale changer: Let $R_f/R_1 = K$ (a real constant) in the circuit of Fig. 14.6. The output voltage can be written as

$$v_0 = -Kv_1$$
. (14.14)

Thus the output voltage scale is obtained by multiplying the input voltage scale by -K, called the scale factor. Using precision resistors, accurate values of K can be achieved. The inverting amplifier can then serve as a scale changer. A low voltage can be accurately measured by amplifying the voltage by the scale changer and dividing the amplified voltage by the scale factor.

4. Noninverting amplifier: Figure 14.7 depicts the circuit diagram of a noninverting amplifier. The input voltage v_1 is applied to the noninverting terminal. Since the voltage gain of the OP AMP is infinite, the potential of the point G is also v_1 . The current flowing into the OP AMP is negligible, its input impedance being very large. Hence, applying Kirchhoff's current law at the point G we obtain

or

or

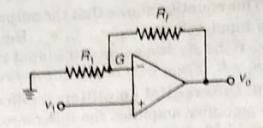


Fig. 14.7 Noninverting amplifier.

$$\frac{v_0 - v_1}{R_f} = \frac{v_1}{R_1} \tag{14.15}$$

 $\frac{v_0}{v_1} = 1 + \frac{R_f}{R_1} \tag{14.16}$

which is the voltage gain of the amplifier system. The voltage gain is greater than unity by a factor R_f/R_1 . As the gain is positive, there is no phase difference between the input voltage v_1 and the output voltage v_0 . The input impedance of the circuit is high and the output impedance is low.

In the circuit of Fig. 14.7, if $R_f=0$ and $R_1=\infty$, the circuit reduces to that of Fig. 14.8. Equation (14.16) shows that the voltage gain in this case is unity. Therefore, the circuit of Fig. 14.8 is referred to as a unity-gain buffer or a voltage follower. This circuit offers a high input impedance and a low output impedance, and therefore can be employed as an impedance matching device between a high-impedanace source and a low-impedance load.

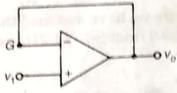


Fig. 14.8 A voltage follower.

Figure 14.9 gives the circuit diagram of an adder or a summing amplifier. The same reasoning as in the case of the inverting amplifier shows that the point G is a virtual ground, i.e. G is at ground potential. The input impedance of the OP AMP being infinite, the sum of the currents $i_1, i_2, ..., i_n$ will be equal to i_0 , by Kirchhoff's current law. That is,

Fig. 14.9 Summing amplifier

 $i_{1} + i_{2} + \dots + i_{n} = i_{0}$ or $\frac{v_{1}}{R_{1}} + \frac{v_{2}}{R_{2}} + \dots + \frac{v_{n}}{R_{n}} = -\frac{v_{0}}{R_{f}}$

 $v_0 = -\left(\frac{R_f}{R_1}v_1 + \frac{R_f}{R_2}v_2 + \dots + \frac{R_f}{R_n}v_n\right)$ (14.17)

If $R_1 = R_2 = ... = R_n = R$, Eq. (14.17) gives

$$v_0 = -\frac{R_f}{R} (v_1 + v_2 + \dots + v_n)$$
 (14.18)

With $R_f = R$, Eq. (14.18) reduces to

$$v_0 = -(v_1 + v_2 + \dots + v_n). \tag{14.19}$$

This equation shows that the output voltage v_0 is numerically equal to the algebraic sum of the input voltages $v_1, v_2, ..., v_n$. Hence the circuit is termed a summing amplifier or an adder. If the algebraic sum of the input voltages is very small, the output voltage v_0 is measured with $R_f > R$. From Eq. (14.18), the desired sum is obtained accurately by dividing v_0 by R_f/R_1 .

6. Differential amplifier: A differential (or difference) amplifier amplifies the difference of two voltages. Figure 14.10 shows the circuit diagram of a differential amplifier. Suppose that the difference between the voltages v_2 and v_1 is to be amplified. The voltage v_2 is applied to the noninverting input terminal and v_1 to the inverting input terminal of the OP AMP. The output voltage is v_0 . The voltage gain of the OP AMP being infinite, the points a and b will have the same potential, say, v_x . Applying Kirchhoff's current law at a and b, we obtain respectively

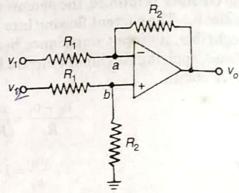


Fig. 14.10 Differential amplifier.

and

$$\frac{v_2 - v_x}{R_1} = \frac{v_x}{R_2} \tag{14.21}$$

where we have assumed that the input impedance of the OP AMP is infinite. Subtracting Eq. (14.20) from Eq. (14.21), we get

(14.20)

$$v_0 = \frac{R_2}{R_1} (v_2 - v_1) \tag{14.22}$$

Thus v_0 is the amplified version of the difference voltage $(v_2 - v_1)$, the voltage gain of the amplifier system being R_2/R_1 .

7. Oscillator: Owing to its high gain and wide bandwidth, the IC OP AMP can be used in oscillator circuits. Figure 14.11 shows the circuit diagram of a phase-shift RC oscillator using an OP AMP. The RC network is connected at the output of the OP AMP. The resistance R_3 of the potentiometer is greater than R. Also, the feedback resistance R_2 is greater than R_1 to achieve a proper voltage gain of the inverting amplifier system. The potentiometer slider is

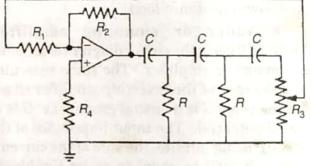


Fig. 14.11 Phase-shift oscillator using OP AMP.

adjusted for unity loop gain. Sustained oscillations at a frequency determined by the network parameters can then be obtained.

The use of an OP AMP as the active element in the Wien-bridge oscillator circuit is shown in Fig. 14.12. The oscillation frequency is $f_0 = 1/(2\pi RC)$. The principle of oscillation has been discussed in detail in Chapter 11. From Eq. (11.58) we find that the voltage gain A of the active element must be δ , where δ (a positive number greater than 3) is given by Eq. (11.54).

8. Differentiator: The circuit of Fig. 14.13 gives an output voltage v_0 which is proportional to the derivative of the input voltage v_1 with respect to time. Therefore, the circuit is termed a differentiator. The infinite voltage gain of the OP AMP makes G a virtual ground. The charge on the capacitor C is therefore $q = Cv_1$

$$v_1 = \frac{q}{C}. (14.23)$$

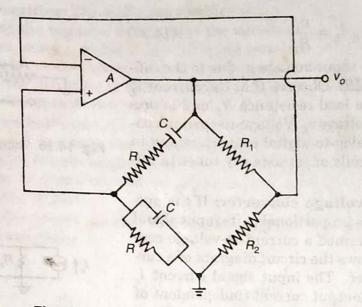
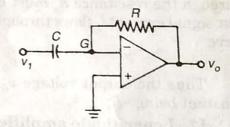


Fig. 14.12 Wien-bridge oscillator using OP AMP.

Differentiating with respect to time, we obtain

$$\frac{dv_1}{dt} = \frac{1}{C} \frac{dq}{dt} = \frac{i}{C} \tag{14.24}$$

where i is the current flowing through the capacitor. Since the input impedance of the OP AMP is infinite, the current i flows through the resistance R also. Therefore, $i = -v_0/R$, so that Eq. (14.24) gives



$$v_0 = -CR \frac{dv_1}{dt}$$
 (14.25)

Fig. 14.13 Differentiator.

Obviously, the output voltage v_0 is proportional to the time derivative of the input voltage v_I , the proportionality constant being -CR.

9. Integrator: If the positions of R and C in the circuit of Fig. 14.13 are interchanged, the resulting circuit, depicted in Fig. 14.14, is an integrator. As the gain of the OP AMP is infinite, the point G is a virtual ground. The current i flowing through the resistance R is $i = v_1/R$. The input impedance of the OP AMP being infinite, the current i flows through the feedback capacitor C to produce the output voltage v_0 . Therefore,

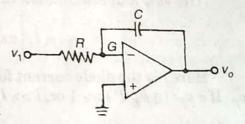


Fig. 14.14 Integrator.

$$v_0 = -\frac{1}{C} \int_0^t i \, dt = -\frac{1}{CR} \int_0^t v_1 \, dt \,. \tag{14.26}$$

The output voltage v_0 is thus proportional to the time integral of the input voltage v_I , the proportionality constant being -1/(CR). Hence the circuit is referred to as an *integrator*. Integrators find applications in sweep or ramp generators, in filters, and in simulation studies in analog computers.

10. Voltage-to-current converter: If the output current of a device is proportional to its input signal voltage, the device is called a voltage-to-current converter. The noninverting amplifier circuit of Fig. 14.7, redrawn in Fig. 14.15, can serve as a voltage-to-current converter, the load resistance R_L replacing the resistance R_f . If i_L is the current through R_L , we have

$$i_L = \frac{v_1}{R_1}$$
 (14,27)

the point G having the input voltage v_1 due to the infinite gain of the OP AMP. Observe that the current i_L does not depend on the load resistance R_L and is proportional to the input voltage v_1 . Voltage-to-current converters are used in analog-to-digital converters and in driving the deflection coils of cathode ray tubes in television.

11. Current-to-voltage converter: If the output voltage of a device is proportional to its input signal current, the device is termed a current-to-voltage converter. Figure 14.16 shows the circuit diagram of a current-to-voltage converter. The input signal current i_g can be provided by the output current (independent of the load) of a photocell or a photomultiplier tube. Since the point G serves as a virtual ground, the current through the resistance R_g must be zero. The whole in-

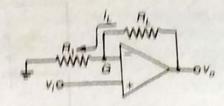


Fig. 14.15 Voltage-to-current converter.

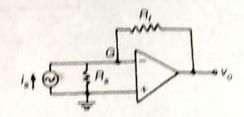


Fig. 14.16 Current-to-voltage converter.

put signal current i_s flows through the feedback resistor R_f to produce the output voltage v_0 . We have

$$v_0 = -i_s R_f \tag{14.28}$$

Thus the output voltage v_0 is proportional to the input current i_s , the proportionality constant being $-R_c$

12. Logarithmic amplifier: If the feedback resistor R_f in the circuit of Fig. 14.6 is replaced by a diode, we obtain a *logarithmic amplifier* giving an output voltage v_0 that changes as the logarithm of the input voltage v_1 . The circuit of a logarithmic amplifier is shown in Fig. 14.17.

The volt-ampere characteristic of the diode is given by Eq. (5.5), viz.

$$i = I_{\rm B} \left[\exp \left(\frac{ev_f}{\eta k_B T} \right) - 1 \right]$$

Here i is the diode current for the forward voltage v_f . If $e \, v_f / (\eta \, k_B \, T) >> 1$ or, $i >> I_a$, we have

$$i = I_s \exp\left(\frac{ev_f}{\eta k_B T}\right)$$

or,
$$\ln\left(\frac{i}{I_s}\right) = \frac{ev_f}{\eta k_B T}$$

or,

$$v_f = \frac{\eta k_B T}{e} \ln \left(\frac{i}{I_s} \right)$$

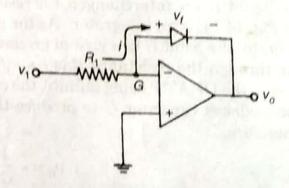


Fig. 14.17 A logarithmic amplifier for positive input voltage v_1 .

Since G is a virtual ground in Fig. 14.17, we have $i = v_1/R_1$ and the output voltage is

$$v_0 = -v_f = -\frac{\eta k_B T}{e} \ln \left(\frac{v_1}{I_s R_1} \right).$$

Hence v_0 responds to the logarithm of v_1 .

13. Half-wave rectifier: The half-wave rectifier circuit of Fig. 14.18 operates in the 64. During the negative half cycle of the sinusoidal input voltage v_i (Fig. 14.19), lower manner. During the negative half cycle of the inverting terminal of the OP AMP. Now, D_1 in the voltage v is positive, since v_i is fed to the inverting terminal of the OP AMP. Now, D_1 in the voltage v is positive, as shown in Fig. 14.19. Thus $v_0 = -(R_2/R_1)v_i$. The amplified resistance, the gain of the inverting amplifier is $-R_2/R_1$. Thus $v_0 = -(R_2/R_1)v_i$. The amplified resistance, the gain of the inverting amplifier is $-R_2/R_1$. Thus $v_0 = -(R_2/R_1)v_i$. The amplified resistance, the gain of the inverting amplifier is $-R_2/R_1$. Thus $v_0 = -(R_2/R_1)v_i$. The amplified resistance is positive, as shown in Fig. 14.19.

puring the positive half-cycle of v_0 , D_1 is OFF and D_2 is ON. Again neglecting the diode puring the positive half-cycle of v_0 , D_1 is OFF and D_2 gives a virtual ground at the resistance, we find $v_0 = 0$ (because the feedback through D_2 gives a virtual ground at the inverting input). Clearly, the circuit gives half-wave rectification. The important features are inverting input). Clearly, the circuit gives half-wave rectification. The important features are that amplification occurs together with rectification and that rectification is achieved at that amplification observed that applied to about 100 kHz.

A full wave rectifier circuit can also be obtained using OP AMPs and diodes. The details are not given here for simplicity.

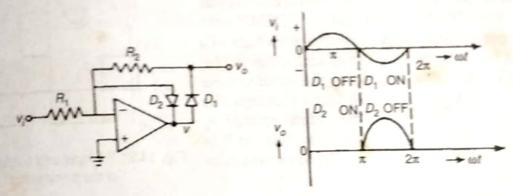


Fig. 14.18 A half-wave rectifier.

Fig. 14.19 Waveforms of v₀ and v₁

14. Peak detector: In the peak detector circuit (Fig. 14.20), if the input voltage v_i is larger than the output voltage v_0 , the OP AMP output voltage v is positive. Hence the diode D is forward biased and it conducts. The circuit now acts as a voltage follower, so that $v=v_i$, and the capacitor C is charged by the amplifier output current through D to the voltage v_i . If v_i now drops below the capacitor voltage v_0 , the OP AMP output voltage v is negative and the diode D turns OFF. The capacitor cannot discharge, and holds at any instant of time t the most positive value of the input voltage v_i prior to t (Fig. 14.21). After the operation, the circuit is reset by activating the gate of a MOSFET connected across the capacitor. The MOSFET acts as a switch to discharge the capacitor.

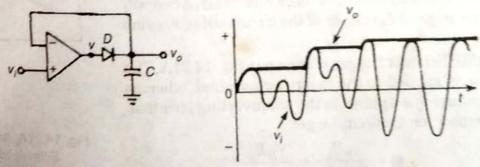


Fig. 14.20 Peak detector

Fig. 14.21 Input and output voltage waveforms.

15. Voltage comparator: A voltage comparator (or simply a comparator) is a device used for the comparison of two voltage levels. The output of the comparator indicates which of the two input voltages is greater. Hence it is a switching device, giving an output voltage when one

input voltage is larger, and another output voltage when the other input voltage is larger. An GP AMP can be used as a comparator by operating it in the open-loop condition and applying the two voltages to be compared to the inverting and the noninverting inputs. If the voltage to the noninverting input terminal (v_1) slightly exceeds the voltage to the inverting input terminal (v_2) , ceeds the voltage to the inverting input terminal (v_2) , ceeds the voltage to the inverting input terminal (v_2) , ceeds the voltage V, and if v_2 is slightly greater than v_1 , output voltage V, and if v_2 is slightly greater than v_1 , voltage V. This behaviour results from the very large voltage -V. This behaviour results from the very large open-loop gain, and is illustrated in Fig. 14.5C. The output voltage v_0 switches when $v_d = v_1 - v_2 = 0$.

To further clarify the behaviour of the comparator we show in Fig. 14.21(i) an open-loop OPAMP with supply voltages +V and -V. A dc source of voltage $+V_R$ is connected to the inverting input and a sinusoidal voltage $v_i = V_m$ sin ωt is applied to the noninverting input $(V > V_m > V_R)$. Figure 14.21(ii) displays the comparator output voltage v_0 . The output voltage v_0 switches to +V whenever v_i exceeds V_R . v_0 stays at V as long as $v_i > V_R$. When v_i drops below V_R , the comparator output switches to -V.

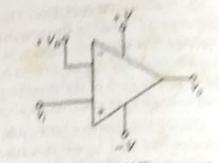


Fig. 14.21 (I) An OP AMP comparator

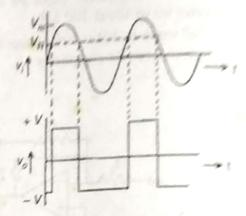


Fig. 14.21 (ii) Input and output voltages of the comparator.

Sometimes the inverting or the noninverting input terminal is grounded. The comparator then acts as a zero-crossing detector. If the inverting input is grounded, the output voltage v_i switches to the maximum positive voltage V when the voltage v_i to the noninverting input is slightly positive. When v_i is slightly negative, v_0 switches to -V. If the noninverting input is grounded, the reverse action takes place.

14.8 THE SCHMITT TRIGGER

With a positive or regenerative feedback, an OP AMP circuit can be constructed to switch from one voltage level to another, showing the phenomenon of hysteresis or backlash. Such a circuit is called a regenerative comparator, or more commonly, a Schmitt trigger after the original developer of the circuit using vacuum tubes.

An OP AMP Schmitt trigger is shown in Fig. 14.21A. The input voltage v_i is applied to the inverting terminal, whereas the feedback voltage v_f is applied to the noninverting terminal. From the superposition theorem we get

$$v_f = \frac{v_0 R_1}{R_1 + R_2} + \frac{V_R R_2}{R_1 + R_2}$$

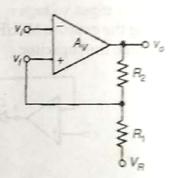


Fig. 14.21A An OP AMP Schmitt trigger.

If v_i is small or negative such that $v_i << v_p$ then the amplifier will saturate giving $v_0 = V_A$, where V_A is the positive saturation voltage. So,

$$v_f = \frac{V_A R_1}{R_1 + R_2} + \frac{V_R R_2}{R_1 + R_2} = V_1 \text{ (say)}.$$

Interested Circuits and Operational Amplifuers

the new marries of in the positive direction. Then on where we have W. At this remains the threshold, the switches recommendated and the comput where the property of $v_0 = -V_{A'}$. This is This is not seen to describe V_{μ} to and hence v_{μ} will decrease. to decrease to further. This cumulative The bolt of The where we are the transfer as $v_{\parallel} > V_{\parallel}$ THE Shows the transfer characteristic

THE ST. WE DAY

$$x_0 = \frac{W_{R1}R_{22}}{R_1 + R_2} - \frac{W_{R1}R_{21}}{R_2 + R_2} = W_{21} \text{ (say)}.$$

The satisfact action occurs only if the amplification is second large of the small changes in 1, are amplified to the description. The fe-discrete factor here $\pi(B = R_1/R_1 + R_2)$. The mount will function satisfactorily provided the loop gain - H. Harris berne floor unity

Some fire we now decrease v. Then the output will The Ty A representative transition will occur in the point is flown in Fig 14.21B(b) so that 10 will switch

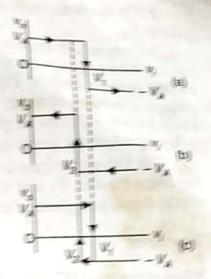


Fig. 14.213 Transfer diaracteristic of the Schmitt trigger for (a) increasing w, and (b) decreasing w. (d) The overall imput-output curve exhibiting hysteresis.

mental entry. The overall transfer characteristic of the Schmitt trigger is depicted mile 12 Bc. The curve is called a bysterents curve because it has the form of a magnetic involves into The hydreresis curve shows that the discuit triggers at a higher voltage for present must be the for becreasing input signals.

The with of the hysteress loop is given by

$$V_{\pm} = V_1 - V_2 = \frac{2R_1 V_4}{R_1 + R_2}$$

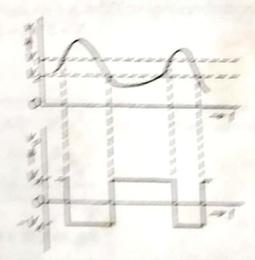
In order to reduce V_H , we have to make $R_i(R_1+R_2)$ small. But it cannot be reduced greatly for otherwise the may gain. Let, becomes small

Surprise we have to design a Delmitt trigger ther which War a W, and War LAS W, uning an THE SUPPLY WHITE WEST VEST Ly = 20000, Then

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The loss
$$200 \text{ is} - \frac{A_0 \text{ E}_0}{\text{E}_0 \text{ E}_0} = 2000 \times 3 \times$$

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Electronics-Fundamentals and Applications

 $V_2 = 2.976 \text{ V}$. Note that these trigger voltages are primarily determined by the relative voltage V_R .

An important application of the Schmitt trigger is to transform a slowly varying input voltage into a square wave voltage at the output. Consider the input signal v of Fig. 14.200 plotted against time t. This signal is arbitrary but extends beyond V_1 and V_2 . The output voltage v_0 swings abruptly to $-V_A$ when the input voltage v_1 exceeds V_1 and to $+V_A$ when V_2 and V_3 drops below V_3 . The output voltage is thus a square wave of peak values $+V_A$ and $-V_A$ independent of the amplitude of the input voltage.

The Schmitt trigger is a comparator because the circuit compares an input voltage with the trigger levels V_1 and V_2 for the output voltage to swing between $-V_A$ and $+V_B$. It is a regenerative comparator because it employs positive or regenerative feedback.

Observation

When a practical OP AMP is connected as an amplifier with a closed loop gain, say, A, and an input dc voltage of 1 volt is applied, the output voltage is expected to be A, volt. In practice, the output voltage does not at once attain the final value of A, volt, but takes some time to reach it owing to the inherent internal time constants of the OP AMP. The time rate of change of the closed-loop amplifier output voltage is called the slew rate of the OP AMP. It is a figure of merit, measured in volt per microsecond. A typical value of the slew rate for a monolithic OP AMP is 1 V/ μ s.